a polyphase clock generator for generating multiple clock phases for spreading the samplers in time;

at least one logic device for comparing signals latched by said samplers;

a controller for identifying the position in time at which the BER function is minimal; and

a multiplexor for choosing a signal copy having the minimal BER.

2. The receiver according to claim 1, wherein the sampling system comprises a plurality of samplers producing a series of copies simultaneously.

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3. The receiver according to claim 1 wherein the controller identifies the position in time by continuously measuring and storing values corresponding to minimums of BER function.

4. A receiver for high speed data interconnect, comprising:

a sampling system for receiving a digital signal, comprising a plurality of samplers coupled with a set of delays, for providing a series of signal copies with each copy being shifted by a predetermined time interval, and each signal copy having a Bit Error Rate distribution;

CONT

a clock generator for generating clocks for clocking the samplers;

a logic network for comparing signal copies latched by samplers;

a controller for identifying the position in time at which the BER function is minimal to determine the number of the signal copy with minimal BER;

a multiplexor for choosing the signal copy with minimal BER.

5. The receiver according to claim 4, wherein the plurality of samplers comprises one sampler coupled to a set of delays or a variable delay, for providing a series of spaced in time signal copies.

6. The receiver according to claim 4, wherein the plurality of samplers comprises several samplers coupled to a set of delays, for providing a plurality of spaced in time signal copies, with majority network at the output.

7. The receiver according to claim 4, wherein the signal copies are spaced in time by fixed delays.

8. The receiver according to claim 4, wherein the signal copies are spaced in time by variable delays.

9. The receiver according to claim 6, wherein the signal copies are spaced in time uniformly.

10. The receiver according to claim 4, wherein said delays are incorporated in a data path, in a clock signal path, or in both paths.

11. The receiver according to claim 4, wherein the number of samplers per bit is from 14 to 20, preferably, 16.

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12. The receiver according to claim 4 wherein the controller identifies the position in time by continuously measuring and storing values corresponding to minimums of BER function.

13. The receiver according to claim 4, wherein at least one signal copy from the sampler is used to generate a feedback to control a source of threshold voltage to balance the number of ones and zeros in the sampled data.

14. A receiver for high speed data interconnect, comprising:

at least one sampler for receiving a digital signal, coupled with a set of delays, or a variable delay, for providing a series of spaced in time signal copies, each signal copy having a BER distribution,

CONT

a clock generator for generating clocks for the sampler or samplers;

a logic network for comparing signal copies and selecting a signal copy with minimal BER,

a means to determine the bit errors against the delay,

a means to determine the delay corresponding to a copy with minimal bit error; and

a means to apply the delay determined thereby to other samplers.

15. The receiver according to claim 14, wherein the sampler is implemented as a register, flip-flop, latch, sample-hold, or track-and-hold device.

16. The receiver according to claim 14, wherein the sampler latches data at a point where the BER function has its minimum.

17. The receiver according to claim 14, wherein said delays are incorporated in a data path, in a clock signal path, or in both paths.

18. The receiver according to claim 14, further comprising a pipeline of latency adjustment elements.

19. The receiver according to claim 14, wherein the logic network comprises at least one majority element for providing a value Q, where Q is the value at the majority of its inputs, and a number E, where E is the number of its inputs having value different from the value at the majority of inputs, the minimum number of inputs at the majority element being 3.

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20. A method of high speed data interconnect, comprising the steps of:

receiving a digital signal using a plurality of samplers for sampling data at multiple clock phases, for providing a series of signal copies, each signal copy having a Bit Error Rate Distribution;

comparing signals latched by said samplers;

continuously tracking the minimum of BER distribution to identify the position in time at which the BER function is minimal to choose a signal copy with minimal BER;

selecting a sample with the lowest BER.

CONT

21. A method according to claim 20, wherein a series of simultaneous signal copies is provided.

22. A method according to claim 20, wherein a series of spaced in time signal copies is provided.

23. A method of high speed data interconnect, comprising:

receiving a digital signal using a plurality of samplers for sampling data coupled with a set of delays, for providing a series of signal copies, with each copy being shifted by a predetermined time interval, each copy having a Bit Error Rate Distribution;

comparing signals latched by said samplers;

continuously monitoring the minimum of BER distribution to identify the position in time at which the BER function is minimal;

choosing a signal copy with minimal BER.

24. The method according to claim 23, wherein the minimum of BER distribution is monitored by continuously scanning a variable delay at the input of a transition detector.

25. The method according to claim 23, wherein the sampler that is closest to the minimum in BER function is chosen as the sampler used for data receiving.

26. A method of high speed data interconnect, comprising :

providing at least one sampler for receiving a digital data, coupled with a set of delays or a variable delay;

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generating clock for clocking the sampler or samplers at predetermined time intervals to provide a series of spaced in time signal copies, each signal copy having a Bit Error Rate Distribution;

comparing signal copies to select a signal copy with minimal BER;

determining the bit errors against the delay,

determining the delay corresponding to a copy with minimal bit error; and

applying the delay determined thereby to other samplers so that the step of sampling data is performed at a time corresponding to the delay determined thereby.

CONT

27. The method according to claim 26, wherein the minimum of BER distribution is selected by continuously scanning a variable delay at the input of a transition detector.

28. The method according to claim 26, wherein at the end of each cycle of scanning the variable delay, the co-ordinate of the value closest to the minimum is loaded into one of delays at the input of the sampler.

29. The method according to claim 26, wherein each sampler takes independent samples of their input at different moments of time covering an interval wider than one bit interval.

30. The method according to claim 26, further comprising a step of adjusting latency using a pipeline of latency adjustment elements.

31. A communication channel comprising a plurality of parallel buses, on which a plurality of receivers is arranged, each receiver comprising:

a plurality of samplers for sampling data, providing a series of signal copies, each signal copy having a Bit Error Rate distribution;

a polyphase clock generator for generating multiple clock phases for spreading the samplers in time;

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at least one logic device for comparing signals latched by said samplers;

a controller for identifying the position in time at which the BER function is minimal; and

a multiplexor for choosing a signal copy having the minimal BER.

CONT

32. A communication channel according to claim 31, wherein each receiver comprises a pipeline of latency adjustment elements.

33. A communication channel according to claim 32, wherein initial pipeline values are updated during initialization procedure to provide the same latency on each bit.

This Amendment cancels original claims 1-33 and adds new claims 1-33. Entry and consideration of this Amendment is respectfully requested.

Please note that a co-pending GB application is now under examination in the GB PTO. The amended claims correspond to the claims filed in UK.

A Demand for Preliminary Examination of a corresponding PCT application has been filed timely in EPO. A copy of IPER will be presented upon receipt.

Respectfully submitted,

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